



Features

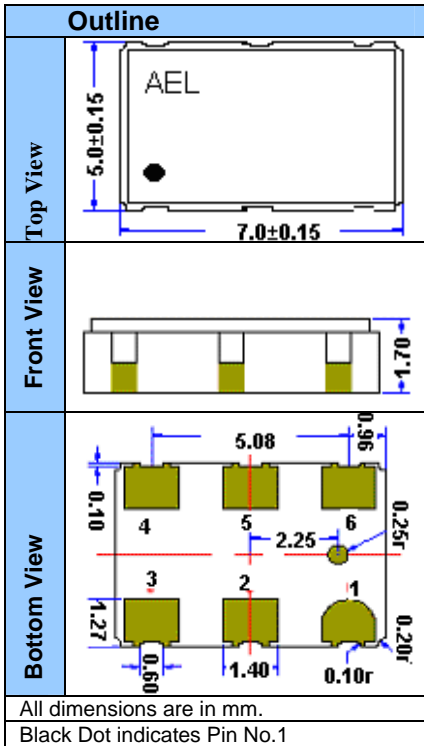
- Frequency 10.9 – 670 MHz
- Package 7X5 mm Ceramic
- LVDS Output
- Low Jitter
- RoHS Compliant Standard
- Supply voltage 3.3v

Table 1

Code	Stability Codes		F	G	M
	Frequency Stability		±20 PPM	±25 PPM	±50 PPM
E	Temperature Range	-10°C to +70°C			
I		-40°C to +85°C			

Denotes Available Denotes not Available

Mechanical Specification



Pin Configuration

Pin	Description
1	Output Enable/Disable
2	No Connect
3	Ground
4	Output
5	Output*
6	Supply

Parameters	Conditions
Series:	XO 590
Frequency Range:	10.9 – 670 MHz
Supply Voltage:	3.3V ± 10%
Output Waveform:	LVDS
Output High Level:	1.60 Volts (max)
Output Low Level:	0.90 Volts (min)
Differential Output (Vod)	250 - 450 mV
Output Offset Voltage (Vos)	1.125 - 1.375 Volts
Differential Output Error(dVos)	50 mV (max)
Output Symmetry	47% - 53% (Referenced to 50% amplitude)
Jitter	0.6 pS RMS (max) 12KHz - 20MHz from Fnominal 2.8 pS RMS (max) 10 Hz - 20MHz from Fnominal
Rise / Fall time:	150 - 230 pS (Vth is20% and 80% of waveform)
Output Short Circuit Current	-20 mA (max) Vout = 0.0 V
Vcc Supply Current:	80mA (max)
Enable/Disable Internal Pull-Up:	50Kohm (min) To Vcc (Equivalent Resistance)
Frequency stability:	(Table 1)Specify
Temperature range:	(Table 1)Specify
V Disable:	0.8Volts (max) Referenced to Ground
V Enable:	2.0Volts (min) Referenced to Ground
Output Leakage:	±20 uA (Vout = Vcc) pad1 low, device disabled ±20 uA (Vout = 0V) pad1 low, device disabled
Enable Time:	10nS (max) Time for output to reach a logic state
Disable Time:	10nS (max) Time for output to reach a high Zstate
Start up time:	5mS (max) Measured from the time Vcc=3.0V
Storage temperature range:	-55°C to +125° C

Specifications subject to change without notice
Revision No. 12b of May 2008

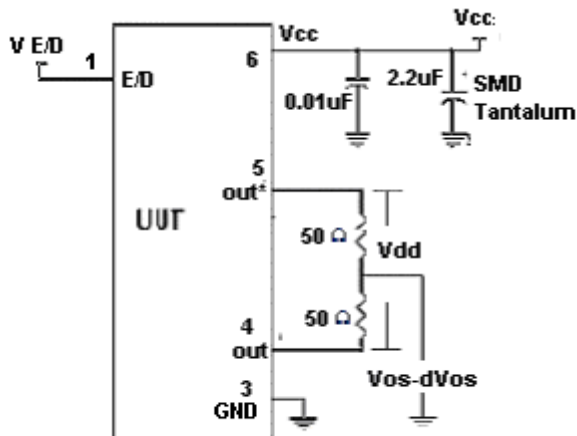
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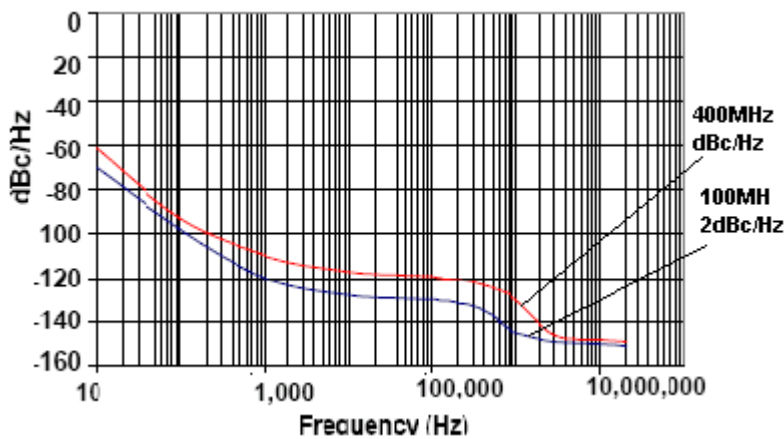
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LOAD CIRCUIT

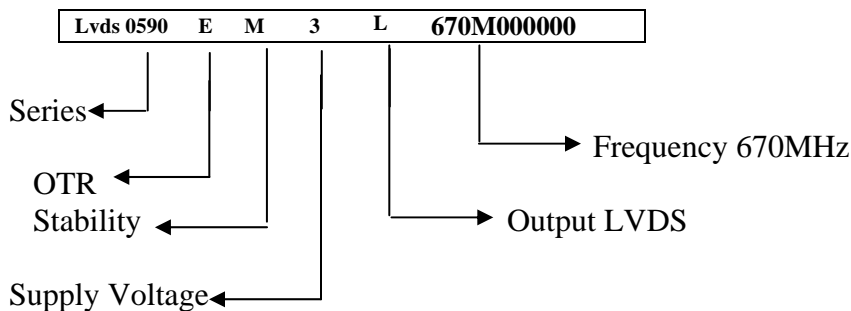


Typical Phase-Noise Response



Ordering Information

Example



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